PVP 14

Code: CS7T4D

IV B.Tech - I Semester – Regular Examinations – October 2017

ADVANCED COMPUTER ARCHITECTURE
(COMPUTER SCIENCE & ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11 x 2 = 22 M

1. a) Define array processor.
   b) What are the applications of Vector Processing?
   c) Define Memory Interleaving.
   d) What is Signed binary?
   e) Write Flynn's classification of computer architecture.
   f) What is Pipelining concept?
   g) Write the basic steps to implement the BOOTH algorithm.
   h) What is meant by COMA model?
   i) Classify the layered development in parallel computers.
   j) What is the purpose of delay insertion?
   k) Define clock cycle.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks. 3 x 16 = 48 M

2. a) What is an Instruction Pipeline? Explain the Instruction pipeline conflicts. 8 M

   b) Explain RISC Pipeline in detail with suitable examples. 8 M

3. a) Draw a flow chart which explains multiplication of two signed magnitude fixed point numbers. 8 M

   b) Explain Restoring division method with an example. 8 M

4. a) Describe the NUMA models for Multiprocessor systems. 8 M

   b) What is Vector Supercomputer? Explain its architecture. 8 M

5. Compare the RISC with CISC scalar Processors. 16 M

6. a) Discuss the models of Linear Pipeline. 12 M

   b) Explain Tomasulo's algorithm. 4 M